

REMARKS

Claims 1-31 and 33-35 are now pending in the application. Claim 34 has been amended to correct a typographical error. Claim 35 has been added. Applicants respectfully traverse and request reconsideration.

Claims 1, 4-11, 13, 15-17, 19, 22-23, 25-28 and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie (U.S. Patent No. 5,859,987) in view of Surugucchi et al. (U.S. Patent No. 6,094,699) and Venkat (U.S. Patent No. 5,857,083).

As to claims 28 and 34, the claims require, among other things, at least one configurable register that includes register configuration logic and at least one register flop to contain an initial value and at least one mask value that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and or writable based on at least one mask value stored in the memory. In the “Response to Arguments” section, the Examiner seems to be misconstruing the claim language. For example, the Examiner relies on Microsoft Press Computer Dictionary second edition 1993 to provide the definition of mask which states “[a] binary value used to selectively screen out or let through certain bits in a data value.” However, the claim is not selectively screening out or letting through certain bits in a data value, rather it is configuring at least one register flop to be either readable and/or read/writable. Applicants can find no mention of register configuration logic that configures at least one register flop to be read and or writable in the cited portions of the aforementioned references. Therefore, reconsideration and withdrawal of the rejection of claim 28 is respectfully requested.

With regard to claim 1, the Examiner admits that Gillespie fails to show, teach, or suggest the data bridge having a read only memory for storing at least initial values and mask values for each ASIC of the plurality of ASICs.

The Examiner suggests that it would be obvious to one of ordinary skill in the art to combine the teachings of Gillespie and Surugucchi et al. to render the data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs in order to consolidate configuration. However, Surugucchi et al. explicitly teach that the BASS control logic unit updates the registers in the second configuration register space (which includes the BASS 1 memory mask) with the values in the first configuration space when the values in the first configuration space are set and/or modified. (See column 8, lines 47-51) Therefore, Surugucchi et al. explicitly teach away from using a read only memory for storing mask values because the BASS control logic would not be able to update a read only memory. Accordingly, it would not be obvious for one skilled in the art to combine the teachings of Gillespie and Surugucchi et al. to render the data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs in order to consolidate configuration.

Venkat fails to cure the deficient teachings of Gillespie and Surugucchi et al. As best understood by Applicants, Venkat discloses a bus interface device for interfacing a secondary peripheral bus with a system having a host CPU and a primary peripheral bus. The bus interface of Venkat enables "virtual integration" of multiple physically distinct peripheral devices so that the collection of devices can function as a single integrated unit. The "virtually integrated" devices can share resources such as a dedicated bus, memory space, and memory bandwidth just as if the devices were physically integrated. An intelligent device configuration process and a dynamic internal memory map allow each peripheral device to be independently added to the system, removed from the system, or upgraded just as if each device was a completely separate peripheral. The bus interface provides a dedicated secondary bus that enables multimedia and graphics bus traffic to be isolated from the CPU's primary peripheral bus. Applicants can find no mention of data bridge having a read only memory for storing mask values for each ASIC of the

plurality of ASICs. Therefore, reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

Claim 10 is allowable for at least similar reasons as claim 1. For example, the references do not teach or suggest forming configurable registers as claimed. Therefore, reconsideration and withdrawal of the rejection of claim 10 is respectfully requested.

Claims 2-9, 11-18, and 34-35 each ultimately depend on claims 1 and 10 and are allowable for at least similar reasons. Claims 2-9, 11-18, and 34-35 are also believed to be allowable for having novel and non-obvious subject matter. Therefore, reconsideration and withdrawal of the rejection of claims 2-9, 11-18, and 34-35 is respectfully requested.

Claim 35 is allowable for at least similar reasons as claim 28. Therefore, reconsideration and withdrawal of the rejections of claim 35 is respectfully requested.


Claims 29-31 each ultimately depend on claim 28 and are allowable for at least similar reasons. Claims 29-31 are also believed to be allowable for having novel and non-obvious subject matter. Therefore, reconsideration and withdrawal of the rejection of claims 29-31 is respectfully requested.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (312) 609-7599.

Respectfully submitted,

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